DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT259
8-bit addressable latch

Product specification
File under Integrated Circuits, IC06

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Philips
Semiconductors

PHILIPS

8-bit addressable latch 74HC/HCT259

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT259 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT259 are high-speed 8-bit addressable latches designed for general purpose storage applications in digital systems. The “259” are multifunctional devices capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q_0 to Q_7), functions are available.

The “259” also incorporates an active LOW common reset ($\overline{MR}$) for resetting all latches, as well as, an active LOW enable input ($\overline{LE}$).

The “259” has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A_0 to A_2) and data (D) input. When operating the “259” as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the “259”.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	D to Q_n		18	20	ns
	A_n, $\overline{LE}$ to Q_n		17	20	ns
t_{PHL}	$\overline{MR}$ to Q_n		15	20	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

8-bit addressable latch | 74HC/HCT259

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5, 6, 7, 9 10, 11, 12	Q_0 to Q_7	latch outputs
8	GND	ground (0 V)
13	D	data input
14	$\overline{LE}$	latch enable input (active LOW)
15	$\overline{MR}$	conditional reset input (active LOW)
16	V_{CC}	positive supply voltage

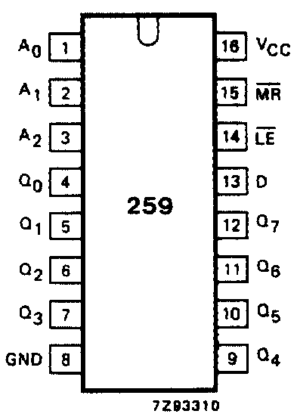


Fig.1 Pin configuration.

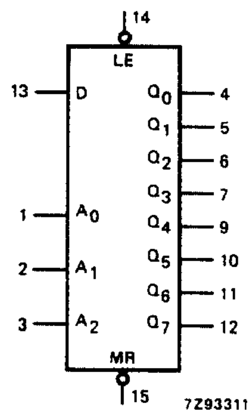


Fig.2 Logic symbol.

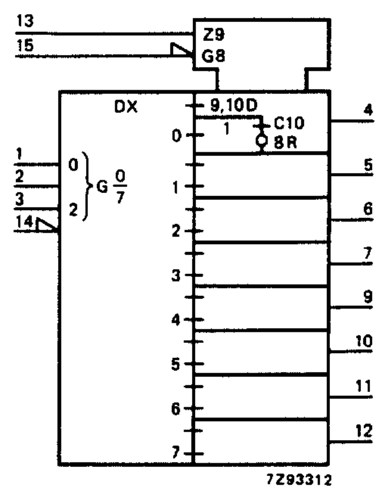


Fig.3 IEC logic symbol.

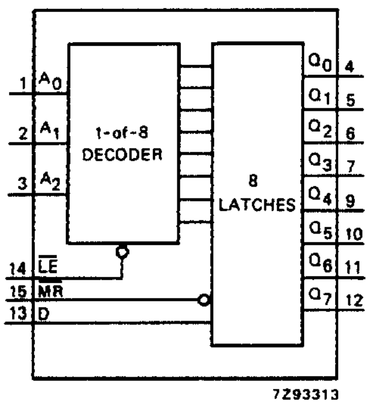


Fig.4 Functional diagram.

MODE SELECT TABLE

$\overline{LE}$	$\overline{MR}$	MODE
L	H	addressable latch
H	H	memory
L	L	active HIGH 8-channel demultiplexer
H	L	reset

FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS							
	$\overline{MR}$	$\overline{LE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
master reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
addressable latch	H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	H	L	q_0	q_1	q_2	Q=d	q_4	q_5	q_6	q_7
	H	L	d	L	L	H	q_0	q_1	q_2	q_3	Q=d	q_5	q_6	q_7
	H	L	d	H	L	H	q_0	q_1	q_2	q_3	q_4	Q=d	q_6	q_7
	H	L	d	L	H	H	q_0	q_1	q_2	q_3	q_4	q_5	Q=d	q_7
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{LE}$ transition
   q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared

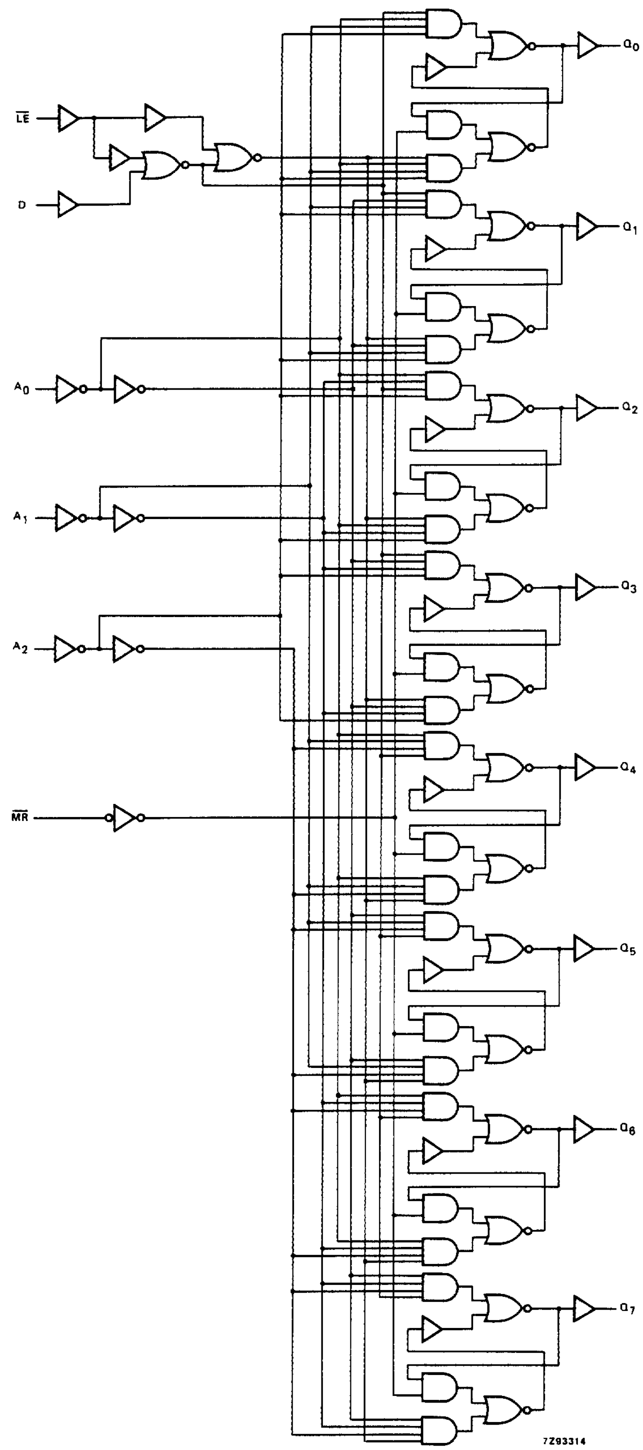


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_{PHL}/ t_{PLH}	propagation delay D to Q_n		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay A_n to Q_n		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to Q_n		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.9
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		119 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
t_W	$\overline{LE}$ pulse width HIGH or LOW	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig.6
t_W	$\overline{MR}$ pulse width LOW	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig.9
t_{su}	set-up time D, A_n to $\overline{LE}$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 10 and 11
t_h	hold time D to $\overline{LE}$	0 0 0	−19 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.10
t_h	hold time A_n to $\overline{LE}$	2 2 2	−11 −4 −3		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.11

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.50
$\overline{LE}$	1.50
D	1.20
$\overline{MR}$	0.75

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 TO +85		−40 TO +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D to Q_n		23	39		49		59	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay A_n to Q_n		25	41		51		62	ns	4.5	Fig.8
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to Q_n		22	38		48		57	ns	4.5	Fig.6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		23	39		49		59	ns	4.5	Fig.9
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7
t_W	$\overline{LE}$ pulse width LOW	19	11		24		29		ns	4.5	Fig.6
t_W	$\overline{MR}$ pulse width LOW	18	10		23		27		ns	4.5	Fig.9
t_{su}	set-up time D to $\overline{LE}$	17	10		21		26		ns	4.5	Fig.10
t_{su}	set-up time A_n to $\overline{LE}$	17	10		21		26		ns	4.5	Fig.11
t_h	hold time D to $\overline{LE}$	0	−8		0		0		ns	4.5	Fig.10
t_h	hold time A_n to $\overline{LE}$	0	−4		0		0		ns	4.5	Fig.11

AC WAVEFORMS

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

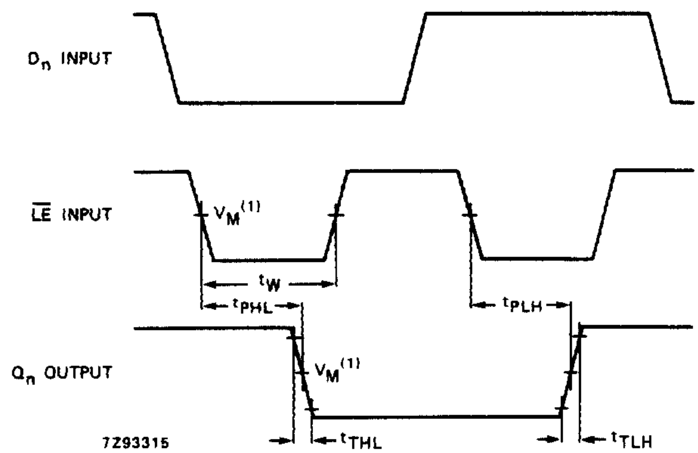


Fig.6 Waveforms showing the enable input ($\overline{LE}$) to output (Q_n) propagation delays, the enable input pulse width and the output transition times.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

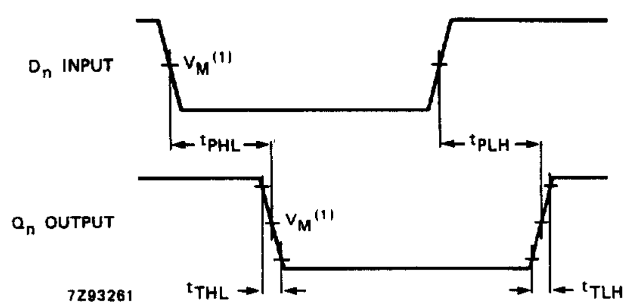


Fig.7 Waveforms showing the data input (D) to output (Q_n) propagation delays and the output transition times.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

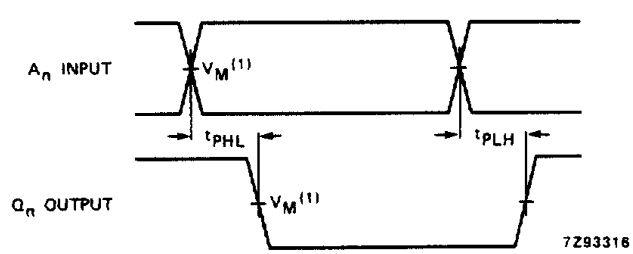
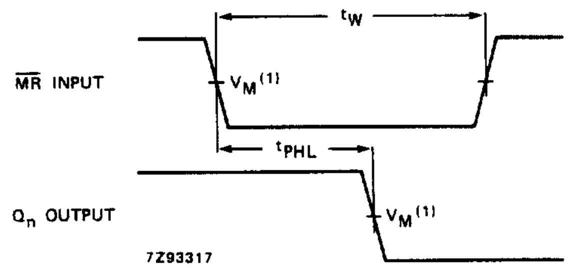
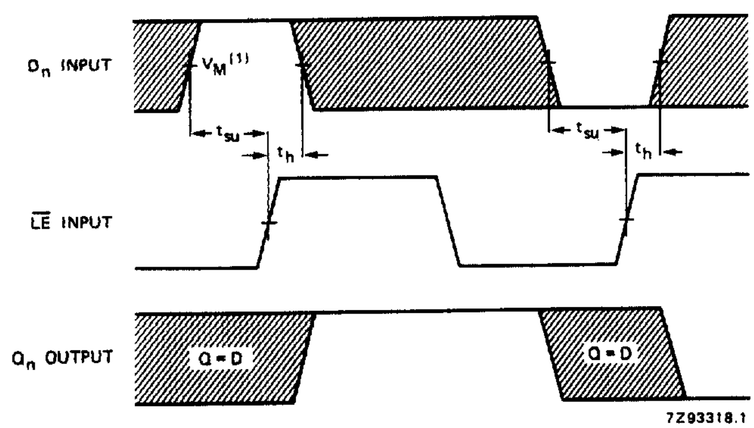


Fig.8 Waveforms showing the address inputs (A_n) to outputs (Q_n) propagation delays and the output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

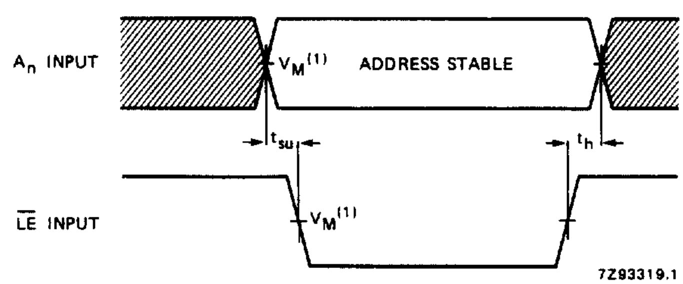
Fig.9 Waveforms showing the conditional reset input ($\overline{MR}$) to output (Q_n) propagation delays.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.10 Waveforms showing the data set-up and hold times for the D input to $\overline{LE}$ input.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.11 Waveforms showing the address set-up and hold times for A_n inputs to $\overline{LE}$ input.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.